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TCAD Simulation of the Electrical Characteristics of Polycrystalline Silicon Thin Film Transistor

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Abstract. Low-temperature polycrystalline silicon thin film transistors (poly-Si TFTs) have been studied because of their high performance in Active Matrix Liquid Crystal Displays (AMLCD's) and Active Matrix Organic Light-Emitting Diode (AMOLED) applications. The purpose of this work is to simulate the impact of varying the electrical and physical parameters (the interface states, active layer's thickness and BBT model) in the transfer characteristics of poly-Si TFT to extract the electrical parameters like the threshold voltage, the mobility and to evaluate the device performance. The device was simulated using ATLAS software from Silvaco, the results show that the electrical and physical parameters of poly-Si TFT affect significantly its transfer characteristics, choosing suitable parameters improve high-performance transistor. Such results make the designed structure a promising element for large-scale electronics applications.

Keywords: poly-Si TFT, transfer characteristics, low temperature, TCAD

Introduction

Amorphous silicon (a-Si) has been principally used as thin film transistors' (TFTs) active layer which has key importance in the fabrication of active matrix liquid crystal displays (AMLCDs) Tseng *et al*. (2002), a-Si:H semi-conductor has been excluded by most manufacturers because of its poor mobility (>1 cm^2 /Vs), degradation under electrical bias stress and instability under illumi-nation (Chang *et al*. 2006; Jahinuzzaman *et al*. 2005; Karim *et al*, 2004; Staebler and Wronski, 1977). Recently, Thin Film Transistors (TFT's) using polycrystalline silicon as an active layer (poly-Si TFT's) have been replacing amorphous silicon thin-film transistors (a-Si TFTs) for their advantages in high field-effect mobility and response time (Bhat *et al*., 1999).

The growing interest in low-temperature poly-Si TFT's applications in flat panel displays (Kim *et al*. 2019; Phong *et al*. 2019; Hu *et al*. 2018) leads us to investigate the effect of interface states, BBT (Band to band tunneling) model and active layer's thickness in the transfer characteristics to evaluate the device performance.

In this paper, a two-dimensional numerical model for the simulation of the transfer characteristics $I_{DS}(V_{GS})$ of poly-Si TFT uses TCAD-ATLAS is developed; the parameters of TFT's model used were obtained from fabricated TFT's using a Silvaco's tool (ATLAS). Our results are a contribution to understand the effect of the inhomogeneity of the active layer of poly-Si TFT on the transfer characteristics I_{DS} (V_{GS}) for a fixed drain bias, they enable us to understand the impact of the granular structure of poly-Si active layer through the pair "thickness-grain size" on the transfer characteristics of poly-Si TFT.

Fabrication process of poly-Si TFTs by Athena module of SILVACO. The first step of the fabrication process of thin film transistor (monolayer) is to cover the substrate with an insulating silicon oxide layer deposited by atmospheric-pressure chemical vapor deposition (APCVD) or Radio Frequency Sputtering (RF sputtering) with a thickness of 0.2 μm (Fig. 1).

The second step allows the opening of the silicon in order to define the gate area. This step includes photolithography with a thickness of 0.1 μm and a width equal to 5 μm, (Fig. 2).

The next step is the deposition of the gate oxide with a thickness of 0.1 μm which corresponds to the gate insulator (Fig. 3).

The last step of the fabrication process is reserved for the definition of the metal contacts of source, gate and drain. The metallization consists of a deposited aluminum layer with a thickness of 0.3 μm followed by a

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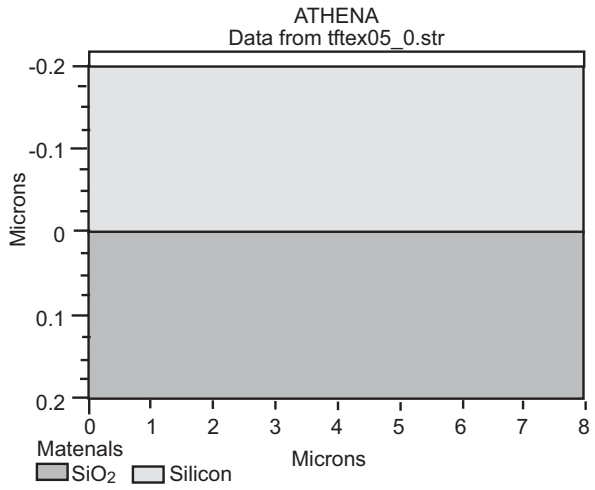

Fig. 1. The obtained structure after silicon deposition using Silvaco's tool (Athena).

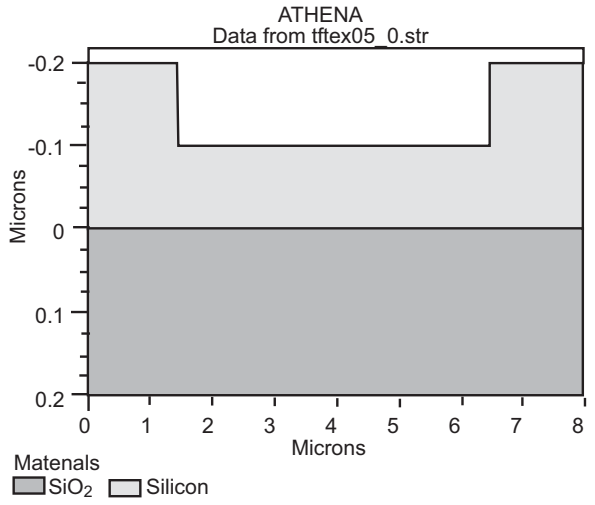

Fig. 2. The structure obtained after the etching of silicon layer using Silvaco's tool (Athena).

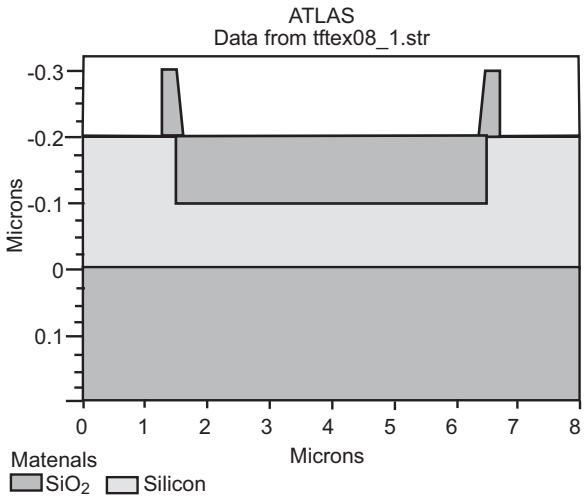

Fig. 3. The structure obtained after oxide's deposition using Silvaco's tool (Athena).

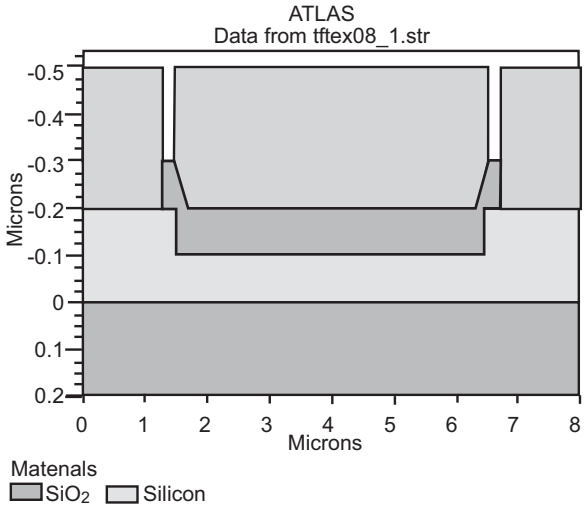

Fig. 4. Structure used for two-dimensional simulation of poly-Si TFT using a Silvaco's tool (Athena).

photolithography step and a step of wet etching of the aluminum layer, this allows defining the contacts (Fig. 4).

Simulation's results of poly-Si TFT uses Atlas module of SILVACO. We can illustrate the transfer characteristics obtained after the simulation by Atlas in the Fig. 5. Negative polarizations of the gate will generate strong electric fields in the channel. Moreover, these polarizations will tend to bend the valence and conduction bands. The curvatures of the bands and the strong fields will thus favor the passage of electrons from the valence band to the conduction band by the tunnel effect, this phenomenon will obviously only occur in the case of weak currents (the blocking state of the transistor).

Effect of interface states on the transfer characteristics. Figure. 6 illustrates the effect of the interface states on the transfer characteristics of poly-Si TFT. In the accumulation regime, the drain current is very little affected by the variation in the quantity and the sign of the interface states. On the other hand,

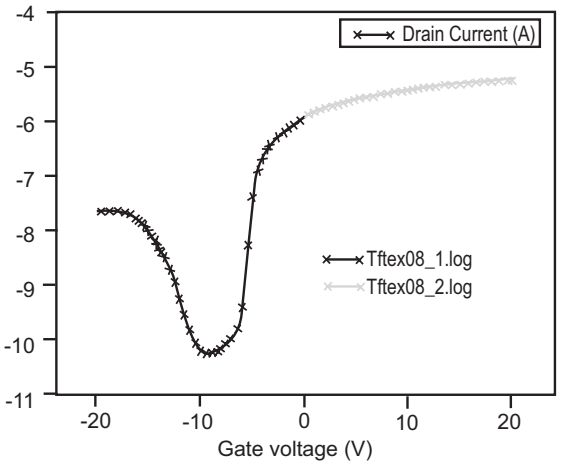

Fig. 5. Variation of drain current I_{DS} as a function of gate voltage V_{GS}.

in the inversion regime, the increase in the quantity of the interface states Qf will increase the current I_{off} significantly. The variation in the sign of the interface states is translated by a shift of the threshold voltage V_T.

Silicon oxide has a very good interface with silicon (Logofatu *et al*. 2011). Otherwise, a silicon oxide obtained by deposition at low temperature contains mobile and fixed charges which influence the quality of the transistor.

Effect of BBT model on the transfer characteristics. We show in the Fig.7, the effect of the phenomenon of an electron passing from the valence band to the conduction band by band to band tunneling (BBT) on the poly-Si TFT transfer characteristics for different values of BBT. If a sufficiently high electric field exists within a device local band bending may be sufficient to permit electrons to tunnel by field emission from the valence band into the conduction band. To implement this effect the tunneling generation rate G_{BBT},

where:

$$G_{BBT} = BB.\ AE^{BB.GAMMA} \exp\left(-\frac{BB.\ B}{E}\right) \quad \ldots\ldots\ldots\ldots\ (1)$$

Here E is the magnitude of the electric field and BB.A, BB.GAMMA and BB.B are user definable parameters that can be set within the input deck ("TCAD Simulation of a Polysilicon Thin Film Transistor For Active Matrix Liquid Crystal Displays").

The results show in Fig.7 that the ratio I_{ON}/I_{OFF} can be reduced by the introduction of the BBT model since the increase of the BBT will decrease the generation of free carriers which imply the decrease of the current I_{OFF} Gundapaneni *et al*. (2012).

Effect of active layer's thickness on the transfer characteristics. The evolution of the drain current I_{DS} as a function of the applied gate voltage V_{GS} for different

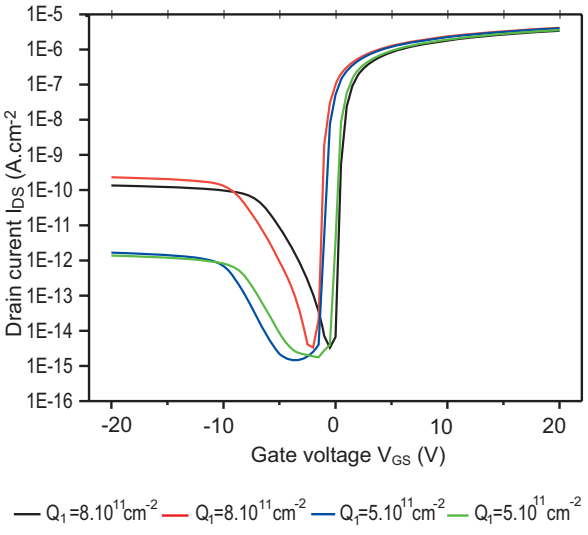

Fig. 6. Sensitivity of poly-Si TFT's transfer characteristics to interface states.

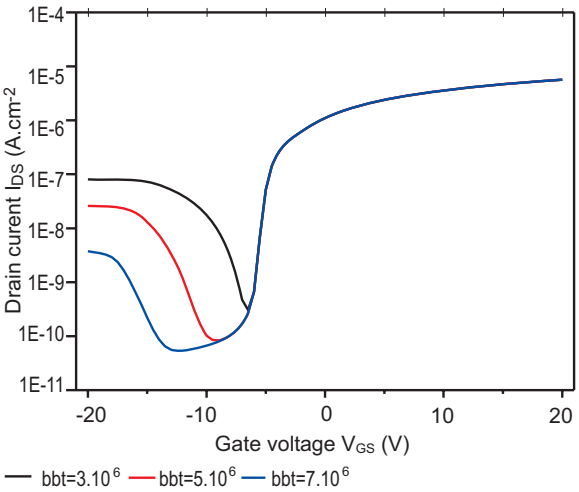

Fig. 7. Sensitivity of poly-Si TFT's transfer characteristics to BBT.

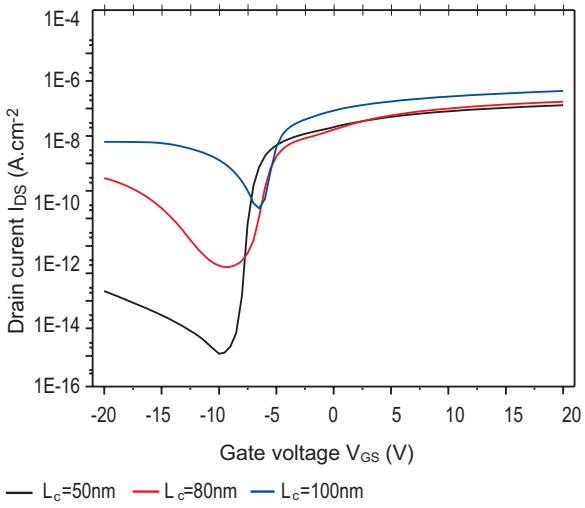

Fig. 8. Sensitivity of poly-Si TFT's transfer characteristics to active layer's thickness.

thicknesses of poly-Si TFT transistor's channel is shown in the Fig. 8.

We were able to confirm that the thinnest active layer gives the best transfer characteristics, as a result of the leakage current resulting from the creation of the carrier currents by tunneling in the channel, this current increases as the active layer's thickness increases.

Figure 9 shows the comparison between simulated and experimental results of Gupta and Tyagi (2006). The

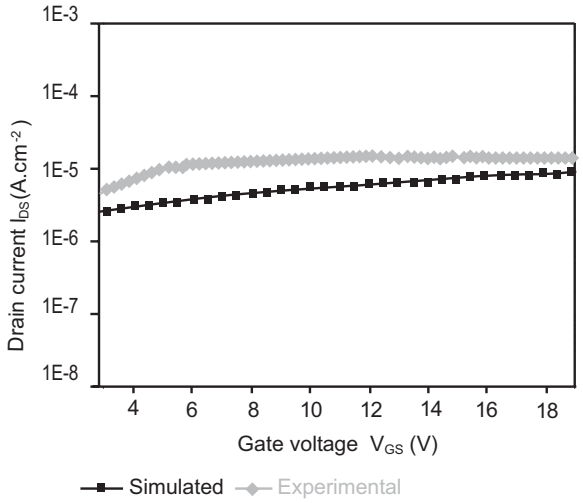

Fig. 9. Drain current I_{DS} as a function of the applied gate voltage V_{GS}, the experimental result of Gupta and Tyagi, (2006) in the red curve and the simulated result in the black curve.

simulated poly-Si TFT's transfer characteristics results show identical trends with experimental variation. However, the deviation from the experimental results is associated with the fact that the experimentally fabricated device may have different density of state value due to different poly-Si material quality Sharma and Gupta (2017).

Conclusion

In this paper, we have established a two-dimensional numerical model for the simulation of the transfer characteristics I_{DS} (V_{GS}) of low-temperature polycrystalline silicon transistors supplied by the electronic component simulator TCAD-ATLAS. The results obtained show that in the accumulation regime (V_{GS}) > 0 the current I_{DS} is little affected by the change of interface states, the thickness of the active layer and the BBT model with its parameters. However, in inversion regime (V_{GS}) < 0, the change of these parameters has a direct impact on I_{OFF} which affect directly the quality of the transistor and degrade the performance of the device. It is clear that the simulation data is in excellent agreement with experimental data from the poly-si TFT device. This paper was proposed to prove the competence of Silvaco software in modeling polysilicon thin film transistors.

Conflict of Interest. The authors declare no conflict of interest

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